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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/066,645	02/06/2002	Scot A. Kellar	042390.P12753	4506

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EXAMINER	
BEREZNY, NEMA O	

ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 05/28/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/066,645	KELLAR ET AL.	
	Examiner	Art Unit	
	Nema O Berezny	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondenc address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *8-11,13-15,17,19 and 20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *8-11,13-15,17,19 and 20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 February 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 4-28-04 has been entered.

Specification

Cancellation of claims 1-7, 16, and 21-26 in paper filed 1-15-04 is acknowledged.

Claim Objections

The objection to claim 13, made in prior Office Action is hereby withdrawn, subsequent to correction made by Applicant in paper filed 1-15-04.

Claim 8 is objected to because of the following informalities: in line 10 after "ILD recess surrounding the" delete "first" and insert --second-- thereto. Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 9, 11, 13 recite the limitation "the metallic lines" in line 2, lines 2-3, and line 3, respectively. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 8-9, 11, and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gupta et al. (2002/0163072) in view of Barth et al. (2003/0003703) and Forouhi et al. (2003/0053081). Gupta discloses a three-dimensional (3-D) integrated chip system, comprising: a first wafer Figs.2-10 el.202) including one or more integrated circuit (IC) devices (el.112), a first plurality of metallic bonding pads (el.114,115) deposited via an interlevel dielectric (ILD) (el.113,116) for wafer-to-wafer bonding and electrical interconnection, and an ILD recess surrounding the first plurality of metallic bonding pads deposited via the ILD (Fig.7); and a second wafer (el.100) including one or more integrated circuit (IC) devices (el.112), a second plurality of metallic bonding pads (el.114,115) deposited via an interlevel dielectric (ILD) (el.113,116) for wafer-to-wafer bonding and electrical interconnection, and an ILD recess surrounding the second plurality of metallic bonding pads deposited via the ILD (Fig.7), and wherein the first plurality of metallic bonding pads is bonded to the second

plurality of metallic bonding pads to establish electrical connections between active IC devices on the adjacent wafers (Fig.8; p.3 para.30). Gupta also discloses the first plurality of metallic bonding pads having a variety of heights and the second plurality of metallic bonding pads having a variety of heights (p.3 para.29), wherein Applicant's specification discloses that the claimed variety of bonding pad heights is a result of etching and/or polishing said pads (p.10 line 16 – p.11 line 6); therefore, it is implied that Gupta would also achieve and disclose the same variety of bonding pad heights during etching (p.3 para.29). Gupta does not disclose a high temperature deformable interlayer dielectric. However, Barth discloses wherein the ILD is a high-temperature deformable SiLK dielectric which exhibits a glass transition near 450 C while the metallic bonding pads exhibit a bonding temperature of about 400 C which is used to allow the bonding areas to be self-leveling to facilitate the bonding of wafers having bonding pads of a variety of heights (p.2 para.18-19). Therefore, it would have been obvious to a person skilled in the art at the time of the invention to use the dielectric of Barth with the IC system of Gupta. The SiLK dielectric of Barth has energy band gaps and extinction coefficients that are sensitive indicators of the curing temperature and time for the curing process (Forouhi - p.1 para.10) **[claims 8, 13]**.

Gupta also discloses wherein the metallic bonding pads include Copper (Cu) bonding pads deposited on opposing surface of the adjacent wafers to serve as electrical contacts between active IC devices on both the adjacent wafers (p.3 para.29) **[claim 9]**; and wherein the ILD recess is created by selectively etching the ILD surrounding the metallic bonding pads deposited via the ILD (p.3 para.29) **[claim 11]**.

Claims 10, 14-15, 17, and 19-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gupta in view of Barth and Forouhi as applied to claim 8 above, and further in view of Desai et al. (5,656,554). Gupta in view of Barth and Forouhi do not disclose wherein the ILD recess is created by a Chemical Mechanical Polish (CMP). However, Desai discloses controlling the solution of a CMP slurry wherein a surrounding dielectric material would be polished or removed at a faster rate than a center conductive/metallic plug (col.4 lines 9-15, 20-38; col.5 lines 6-15). Therefore, it would have been obvious to a person skilled in the art at the time of the invention to use the CMP slurry and procedure of Desai with the IC system of Gupta, Barth, and Forouhi in order to avoid overpolishing or dishing a conductive plug surrounded by dielectric material **[claims 10, 14]**.

As applied to claim 14 above, Gupta also discloses wherein the metallic lines include Copper (Cu) bonding pads deposited on opposing surface of the adjacent wafers to serve as electrical contacts between active IC devices on both the adjacent wafers (p.3 para.29) **[claim 15]**; wherein the ILD recess is created by selectively etching the ILD surrounding the metallic lines deposited via the ILD (p.3 para.29) **[claim 17]**; and wherein the first wafer is thinner than the second wafer to conform to height differences of the metallic lines across opposing surfaces of the adjacent wafers (p.3 para.31) **[claim 20]**.

As applied to claim 14 above, Barth discloses wherein the ILD is a high-temperature deformable SiLK dielectric which exhibits a glass transition near 450

C while the metallic lines exhibit a bonding temperature of about 400 C which is used to allow the bonding areas to be self-leveling to account for height variations across the adjacent wafers to be bonded (p.2 para.18-19). Therefore, it would have been obvious to a person skilled in the art at the time of the invention to use the dielectric of Barth with the IC system of Gupta. The SiLK dielectric of Barth has energy band gaps and extinction coefficients that are sensitive indicators of the curing temperature and time for the curing process (Forouhi - p.1 para.10) **[claim 19]**.

Response to Arguments

Applicant's arguments with respect to claims 8-11 and 13 have been considered but are moot in view of the new ground(s) of rejection.

Applicant's arguments filed 1-15-04 regarding claim 14 (previously claim 16) have been fully considered but they are not persuasive. Applicant contends that the ILD layer of Desai cited by Examiner is actually a sacrificial layer placed over another ILD layer, and is therefore not an ILD layer. Examiner disagrees. An ILD layer is broadly defined as a dielectric material that is formed or placed between metallic layers/lines/pads. Even though the sacrificial layer of Desai performs another function, it still is correctly defined as an ILD layer.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nema O Berezny whose telephone number is (571) 272-1686. The examiner can normally be reached on M-F 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr. can be reached on (571) 272-1702. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

NB

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SUPERVISORY PATENT EXAMINER
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